10.1 A 1.1W/mm²-Power-Density 82%-Efficiency Fully Integrated 3:1 Switched-Capacitor DC-DC Converter in Baseline 28nm CMOS Using Stage Outphasing and Multiphase Soft-Charging

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Over the past years, delivering power to integrated circuits has become increasingly difficult. With the current intake of many modern-day applications growing each new process generation, the Power Delivery Network (PDN) losses have increased as well. By integrating a DC-DC converter together with the load, part of the required voltage conversion can be realized on-chip, and the current intake, together with the PDN losses, can thus ideally be reduced by its Voltage Conversion Ratio (VCR). In order to be viable, though, the converter must 1) have a high efficiency and VCR such that its losses are smaller than the reduction of PDN losses, 2) limit the area overhead by achieving high power density and 3) rely only on commonly available devices to enable wide-spread use.

Switched-Capacitor (SC) converters in particular are a promising candidate for integration. However, the limited monolithic capacitor density has been a burden, causing designs in literature to realize either high efficiency at low power density [1] (94.6% at 1.3mW/mm²) or low efficiency at high power densities [2,3] (60% at 1.1W/mm², 0.77W/mm² respectively). Converters using SOI or Deep-Trench capacitors have improved transistors or >20× higher capacitance density at their disposal, causing them to perform significantly better as a result [4,5], but are more expensive and/or rely on devices that are far from common. Moreover, all of these converters obtain their best result at a VCR of only 3:2 or 2:1, still leaving much room to reduce PDN losses further.

In [1] a technique is introduced that reduces the effective parasitic coupling in SC converters by soft-charging them. In this work, two soft-charging techniques are proposed that significantly *increase* the effective flying capacitance, Cfly, − which is better for high power densities − and get even better with larger VCR.

Figure 10.1.1 compares the presented techniques of Stage Outphasing (SO) and Multiphase Soft-Charging (MSC) to a regular converter for a Dickson topology. In a normal Dickson SC converter, if Vout is close to the technology's Vdd, the top-side switches are usually implemented as 2 stacked standard transistors to avoid using less-efficient I/O devices. This also leads to the creation of intermediate nodes, (k). With SO, each stage is divided into two cells that connect to the same nodes, (k-1) and (k), but run in antiphase. By phase-shifting adjacent stages 90°, a single cell connects to two cells of the adjacent stage over the duration of a (dis)charging state, causing two, rather than one, (dis)charges to occur. For the same total charge transferred, the charge-sharing losses, Pcs, (of charging *and* discharging cells) are subsequently halved. Alternatively, twice the charge can be transferred at the same efficiency, equivalent to doubling Cfly.

MSC is a similar but scalable technique where each intermediate node is split into M separate nodes, (k,1) to (k,M), and a switch is added from each cell to all adjacent nodes. If the charging and discharging cells connect to these nodes in opposite order from one another, the nodes' voltages spread out evenly. With the (dis)charging state consequently split into M equal steps, Pcs is thus divided by M. Because MSC only adds transistors at the top-side, the loss overhead is typically limited and does not outweigh the gain. SO is also fully compatible with MSC: By doubling the number of cells per stage and shifting adjacent stages out-of-phase, a total 2M× reduction of Pcs can be obtained. No soft-charging technique can be applied to (dis)charges of a single capacitor with a fixed DC voltage (e.g. Vout-Vss, Vin-Vout,…). For a Dickson converter, however, there are only two such transfers regardless of the number of stages, making it an excellent topology to use these techniques with for increasing VCR's.

The proposed techniques are implemented in a 3:1 Dickson converter with M=2. Because 2 out of 4 (dis)charges are soft-charged, the effective capacitor density is 60% higher. Figure 10.1.2 gives an overview of the system and phases of this implementation. Rather than using 4M phases, as normally required by MSC+SO, only 6 are needed here due to the fact that both stages only have 3 top-plate connections. Moreover, the availability of 6 phases of which only half is used by each stage, allows the use of the other half for a second core, equalizing the output charge for each phase and reducing the output ripple. In addition, a small decoupling capacitor, equal to 9% of Cfly, was integrated for Vout. A Hysteretic controller, clocked at 1.6GHz and based on [1], regulates the output of the converter.

Cfly is implemented using MOM and MOS capacitors, with I/O devices used in the first stage due to their higher voltage rating. The MOS capacitors (Fig. 10.1.3) are designed with minimal parasitic coupling by using an accumulation capacitor that has a smaller parasitic junction capacitance, Cpwdnw, compared to Cchan thanks to different doping concentrations. Also, a dedicated high-voltage high-impedance bias reduces the junction capacitances and puts them in series, leading to a further reduction of the parasitic coupling. By implementing said impedance as two back-to-back diode-connected PMOS transistors rather than a resistor, which is the usual approach in the literature [7,8], it takes up at least 100 times less area. In simulations, the proposed capacitor has an 18%+ lower parasitic coupling than state-of-the-art [6,7]. While Vbias is not generated on-chip in this work, this can be achieved with minimal area/loss overhead due to its low power requirements (<500nW at 8.5V).

The design is realized in a 28nm baseline CMOS process using a total Cfly of 1.5nF. The measured efficiency versus power density is plotted in Fig. 10.1.4. At the peak power-density of 1.1W/mm², an efficiency of 82% is achieved. Figure 10.1.5 demonstrates the load-transient response of the system. No noteworthy droop nor overshoot were measured without any external load capacitor. This work is compared to the state-of-the-art of high power-density SC converters in Fig. 10.1.6. As can be seen, the presented converter achieves a significantly higher density-efficiency combination than any other baseline CMOS design. Furthermore, thanks to its higher VCR, it is particularly suitable to reduce PDN losses. The chip, shown in Fig. 10.1.7, measures 0.117mm².

This work introduces two soft-charging techniques that significantly increase the effective Cfly for integrated SC converters. A circuit has been fabricated in a 28nm baseline CMOS process that demonstrates the presented techniques and advances the state-of-the-art by achieving a 3:1 conversion ratio with 82% efficiency at 1.1W/mm².

References:

[1] N. Butzen and M. Steyaert, "A 94.6%-Efficiency Fully Integrated Switched-Capacitor DC-DC Converter in Baseline 40nm CMOS using Scalable Parasitic Charge Redistribution," *ISSCC*, pp. 220-221, Jan. 2016.

[2] D. Somasekhar et al., "Multi-phase 1GHz Voltage Doubler Charge-Pump in 32nm logic process," *IEEE Symp. VLSI Circuits*, pp. 196-197, June 2009.

[3] H. Meyvaert, T. Van Breussegem and M. Steyaert, "A Monolithic 0.77W/Mm² Power Dense Capacitive DC-DC Step-Down Converter in 90nm Bulk CMOS," *ESSCIRC*, pp. 483-486, Sept. 2011.

[4] H.-P. Le et al., "Design Techniques for Fully Integrated Switched-Capacitor DC-DC Converters," *IEEE JSSC*, vol.46, no. 9, pp. 2120-2131, Sept. 2011.

[5] T. Andersen et al., "A Sub-ns Response On-Chip Switched-Capacitor DC-DC Voltage Regulator Delivering 3.7W/mm² at 90% Efficiency Using Deep-Trench Capacitors in 32nm SOI CMOS," *ISSCC*, pp. 90-91, Feb. 2014.

[6] J. Jiang et al., "A 2-/3-Phase Fully Integrated Switched-Capacitor DC-DC Converter in Bulk CMOS for Energy-Efficient Digital Circuits with 14% Efficiency Improvement," *ISSCC*, pp. 366-367, Feb. 2015.

[7] H.-P. Le et al., "A Sub-ns Response Fully Integrated Battery-Connected Switched-Capacitor Voltage Regulator Delivering 0.19W/mm² at 73% Efficiency," *ISSCC*, pp. 372-373, Feb. 2013.

[8] G. Villar-Pique, L. Warmerdam, F. Roozeboom, H. J. Bergveld, "Voltage conversion circuit", European Patent EP 2306626A1, publication date June 4th, 2011.

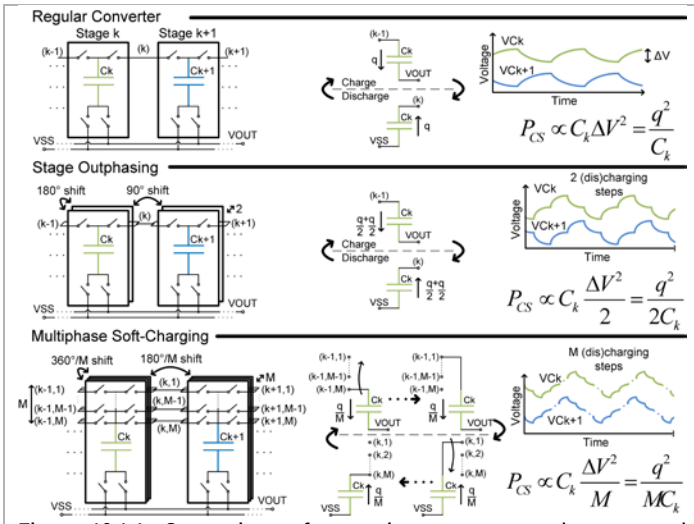

Figure 10.1.1: Comparison of a regular converter to the proposed Stage Outphasing and Multiphase Soft-Charging techniques for a Dickson topology.

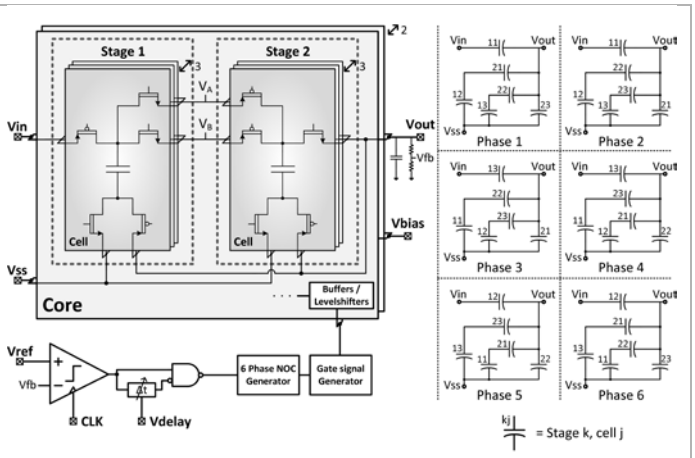

Figure 10.1.2: System overview of the converter with transistor level implementation of the 3:1 converter cores, together with an overview of the converter phases.

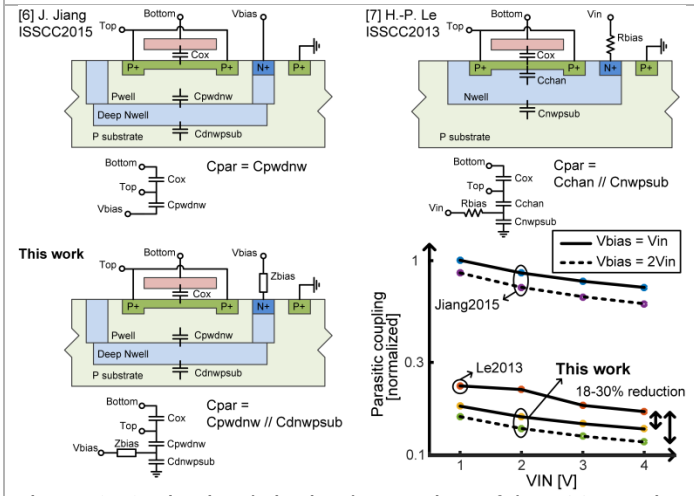

Figure 10.1.3: Visual and simulated comparison of the MOS capacitor implementation used in this work, to state-of-the-art. The proposed implementation has 18%+ lower parasitic coupling.

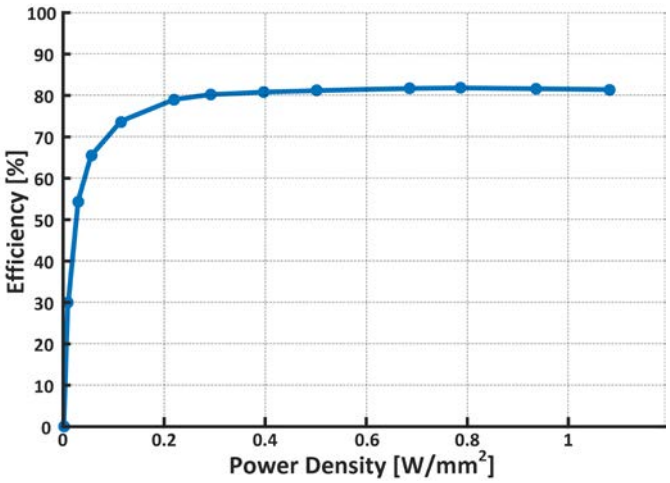

Figure 10.1.4: Measured full-system efficiency versus output power for Vin=3.2V, Vout=950mV and Vbias=8.5V. The converter realizes a peak efficiency of 82% at power densities of 0.65-1.1W/mm².

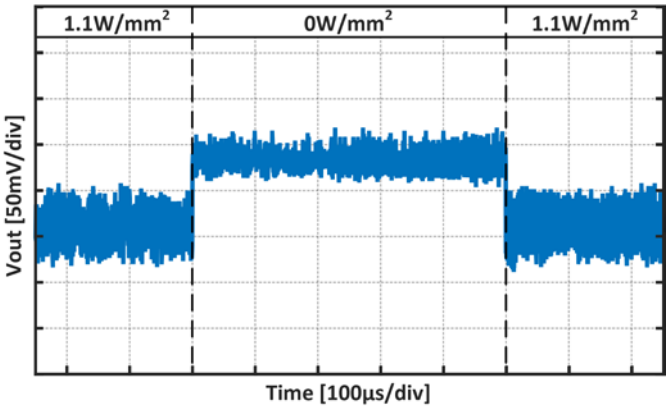

Figure 10.1.5: Measured worst-case load-step transient response with Vin = 3.2V and Vref = 950mV. The converter switches from full load to self-loading operation and back with a transient time of 18ns.

	This Work	[2]	[3]	[4]
Technology	**28nm**	32nm	90nm	32nm SOI
Capacitors	**MOM+MOS**	MOM	MOS	MOM+MOS
VCR_{top} (topology VCR's)	**3:1**	1:2	2:1	3:2 2:1 3:1
Vin [V]	**3.2**	1	2.4-2.6	2
Vout [V]	**0.95**	1.5	0.9-1.3*	0.5-1.15
$P_{D,\,quoted}$ [W/mm²]	**1.1**	1.1	0.77	0.86
η @ $P_{D,\,quoted}$	**82%**	60%	60%	79.8%
Closed Loop?	**Yes**	Yes	No	No
Area [mm²]	**0.117**	0.067	2.14	0.378
VCR_{top} @ $P_{D,\,quoted}$	**3:1**	1:2	2:1	2:1
P_{DCDC}=Ploss/Pload @ $P_{D,\,quoted}$	**22%**	67%	67%	25%
PDN FoM**	**34.5%**	N/A	183.2%	56.0%
High Density FoM [(W/mm²)·1/3]***	**0.37**	1.64	1.83	0.67

*estimate based on graphs

**PDN FoM: $\frac{1-\eta}{\eta - \frac{V_{OUT}}{V_{IN}}}$, lowest normalized PDN losses at which converter still reduces system losses. Lower is better.

***High Density FoM: $\frac{P_{DCDC}}{\sqrt[3]{(1-VCR_{top})^4 P_D}}$, comparison to theoretical limits [4] [M. Seeman Thesis2009]. Lower is better.

Figure 10.1.6: Comparison with Fully Integrated, high power density Switched-Capacitor converters using common capacitor technologies. Baseline CMOS designs are highlighted.

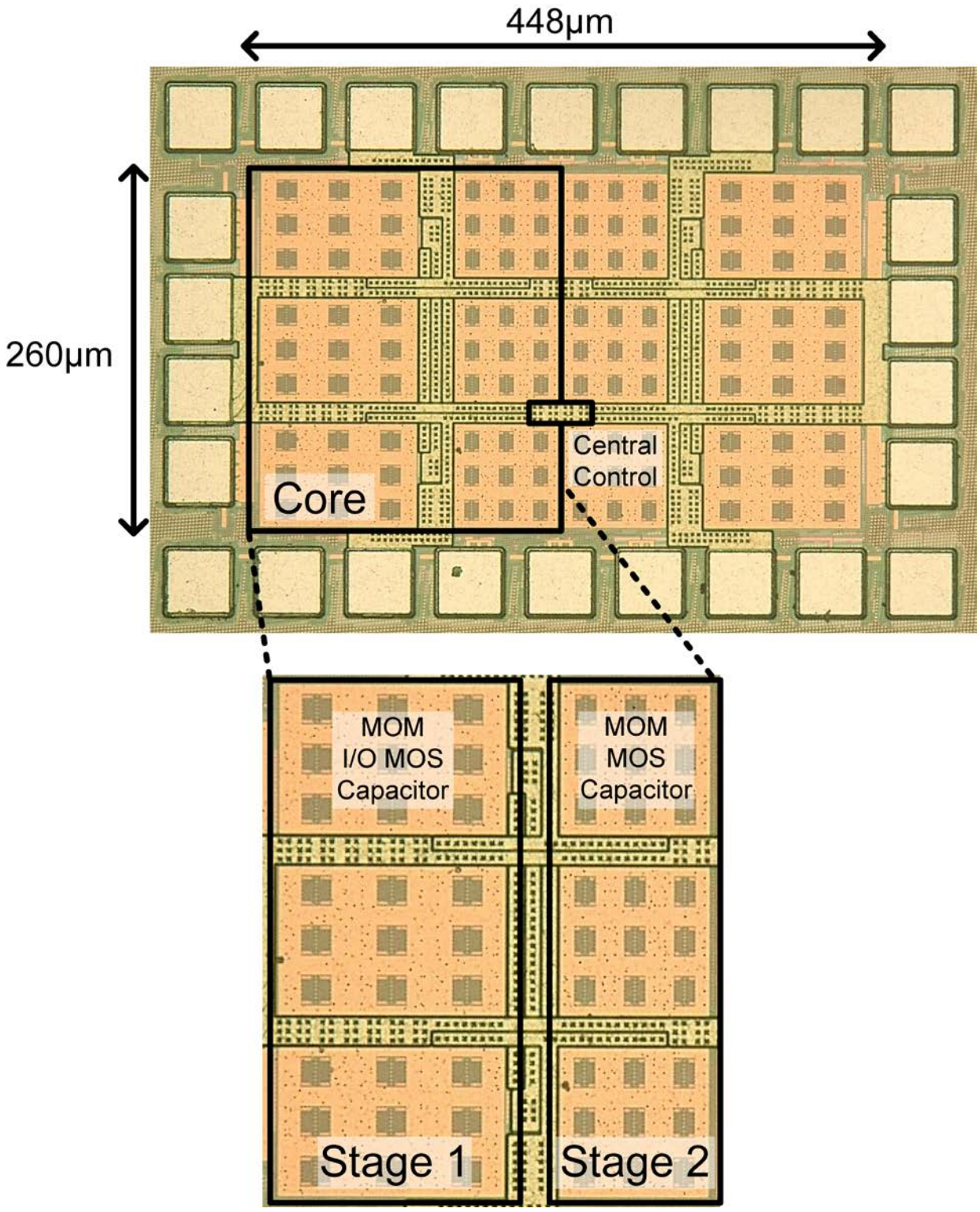

Figure 10.1.7: Die micrograph of measured chip with a total area of 0.117mm^2, excluding bond-pads.